WHAT IS CLAIMED:

1. A structure in a phase changeable memory cell, comprising:

a bottom electrode having an interlayer dielectric layer thereon, the bottom electrode having a recess therein that extends beyond a boundary between the bottom electrode and the interlayer dielectric; and

a phase changeable layer in the recess including a protruding potion of the phase changeable layer that protrudes into the bottom electrode beyond the boundary.

2. A structure according to Claim 1 wherein the recess extends beyond the boundary by a depth to define a side wall of the recess that contacts the protruding portion of the phase changeable layer, wherein the depth is defined to limit an amount of heat transmission from the bottom electrode to the phase changeable layer across the side wall to less than an amount sufficient to cause the phase changeable layer to change phase between a crystalline state and an amorphous state.

3. A structure according to Claim 1 wherein the interlayer dielectric layer includes a contact hole with the phase changeable layer therein on the recess.

4. A structure according to Claim 3 wherein the contact hole has an inward tapered profile extending toward the bottom electrode that defines an opening that is narrower at in the recess than away from the recess.

5. A phase changeable memory cell, comprising:

bottom electrodes disposed over the semiconductor substrate;

a interlayer dielectric layer formed over the semiconductor substrate having the bottom electrodes; and

a plurality of data storage elements extended through the interlayer dielectric layer to connect with the bottom electrodes, respectively,

wherein, each data storage elements is extended into the bottom electrode to predetermined depth so that a portion of the sidewall of the data storage element is contact with the bottom electrode.

6. The phase changeable memory cell of claim 5, further comprising:

a lower interlayer dielectric layer disposed over the semiconductor substrate;

and

storage node plugs extended through the lower interlayer dielectric layer to connect with predetermined region of the semiconductor substrate,

wherein the bottom electrode is formed on the storage node plug to connect with the storage node plug.

7. The phase changeable memory cell of claim 5, further comprising:

a lower interlayer dielectric layer disposed over the semiconductor substrate,

wherein the bottom electrode is extended through the lower interlayer dielectric layer to contact with directly the semiconductor substrate.

8. The phase changeable memory cell of claim 5,

the bottom electrode is formed of one selected form group comprising titanium nitride (TiN), titanium aluminum nitride (TiAlN), titanium silicon nitride (TiSiN), tantalum aluminum nitride (TaAlN) and tantalum silicon nitride (TaSiN).

9. The phase changeable memory cell of claim 5, the data storage element comprising:

a phase changeable pattern electrically connected with the bottom electrode; and

an upper electrode formed on the phase changeable pattern.

10. The phase changeable memory cell of claim 9,

the upper electrode is formed of one selected form group comprising titanium nitride (TiN), titanium aluminum nitride (TiAlN), titanium silicon nitride (TiSiN), tantalum aluminum nitride (TaAlN) and tantalum silicon nitride (TaSiN).

11. A method of forming a structure in a phase changeable memory cell, comprising:

forming a bottom electrode having an interlayer dielectric layer thereon, the bottom electrode having a recess therein that extends beyond a boundary between the bottom electrode and the interlayer dielectric; and

forming a phase changeable layer in the recess including a protruding potion of the phase changeable layer that protrudes into the bottom electrode beyond the boundary.

12. A method according to Claim 11 wherein forming a bottom electrode further comprises:

forming the interlayer dielectric layer on the bottom electrode;

isotropically etching the interlayer dielectric layer to form a mouth of the contact hole having a mouth width; and

anisotropically etching the interlayer dielectric layer though the mouth of the contact hole to beyond the boundary to form the recess in the bottom electrode a recess width that is less than the mouth width.

13. A method according to Claim 11 wherein the recess extends beyond the boundary by a depth to define a side wall of the recess that contacts the protruding portion of the phase changeable layer, wherein the depth is defined to limit an amount of heat transmission from the bottom electrode to the phase changeable layer across the side wall to less than an amount sufficient to cause the phase changeable layer to change phase between a crystalline state and an amorphous state.

14. A method according to Claim 11 wherein the interlayer dielectric layer includes a contact hole with the phase changeable layer therein on the recess.

15. A method according to Claim 14 wherein the contact hole has an inward tapered profile extending toward the bottom electrode that defines an opening that is narrower at in the recess than away from the recess.

16. A method of fabricating a phase changeable memory cell, comprising:

forming a plurality of bottom electrodes on a silicon substrate;

forming a interlayer dielectric layer on the semiconductor substrate having the bottom electrodes;

patterning the interlayer dielectric layer to form a plurality of contact holes exposing a portion of the bottom electrodes, respectively.

etching the bottom electrodes exposed in the contact holes to predetermined

depth; and

forming a plurality of data storage elements on the interlayer dielectric layer, the data storage element is filled in the contact hole and the etched region of the bottom electrode to connect with the bottom electrode.

17. The method of claim 16, wherein forming the contact holes comprising:

isotropic etching a portion of the interlayer dielectric layer to form recess regions over the bottom electrodes; and

anisotropic etching the interlayer dielectric layer at the recess regions to form contact holes exposing a portion of each bottom electrode, respectively,

wherein exposed region of the bottom electrode is formed to an width which is narrower than that of the recess region.

18. The method of claim 16, wherein forming the contact holes comprising:

forming a photo resist pattern on the interlayer dielectric layer, wherein the photo resist pattern is formed to expose a portion of the interlayer dielectric layer over each of the bottom electrodes;

isotropic etching a portion of the interlayer dielectric layer using the photo resist pattern as etch mask to form recess regions;

anisotropic etching the interlayer dielectric layer using the photo resist pattern to form a portion of each bottom electrodes; and

removing the photo resist pattern.

19. The method of claim 16, wherein forming the data storage electrodes:

forming a phase changeable layer, which is filled in the contact hole and the recess regions of the bottom electrodes, over an entire surface of the substrate having the contact holes;

forming a conductive layer on the phase changeable layer;

sequentially patterning the conductive layer and the phase changeable layer to form phase changeable patterns respectively connected with the bottom electrode and upper electrodes over the phase changeable patterns.

20. The method of claim 19, the conductive layer is formed of one selected form group comprising titanium nitride (TiN), titanium aluminum nitride (TiAlN), titanium silicon nitride (TiSiN), tantalum aluminum nitride (TaAlN) and tantalum silicon nitride (TaSiN).

21. The method of claim 16, the bottom electrode is formed of one selected form group comprising titanium nitride (TiN), titanium aluminum nitride (TiAlN), titanium silicon nitride (TiSiN), tantalum aluminum nitride (TaAlN) and tantalum silicon nitride (TaSiN).

22. The method of claim 16, wherein forming the bottom electrodes comprising:

forming lower interlayer dielectric layer over the semiconductor substrate; and

forming a plurality of bottom electrodes extended through the lower interlayer dielectric layer to connect with predetermined regions of the silicon substrate.

23. A method of claim 16 prior to forming the bottom electrode:

forming a plurality of transistors comprising source region, drain region and gate electrode on the semiconductor substrate;

forming a lower interlayer dielectric layer over the semiconductor substrate having the transistors; and

forming storage node plugs extended through the lower interlayer dielectric layer to connect with the source regions, respectively,

wherein the bottom electrode is formed on the storage node plug.

24. A structure in a phase changeable memory cell, comprising:

a bottom electrode having an interlayer dielectric layer thereon; and

a phase changeable layer extending through the interlayer dielectric layer and protruding into a recess in the bottom electrode.